REMARKS

The Applicants respectfully request reconsideration of this application in view of the above amendments and the following remarks.

35 U.S.C. §102(b) Rejection - Abdallah

Claims 19-23, 93-105, 109-120, and 122 have been rejected under 35 U.S.C. §102(b) as allegedly being anticipated by U.S. Patent No. 6,115,812 issued to Abdallah et al. (hereinafter "Abdallah"). The Applicants respectfully submit that the present claims are allowable over Abdallah.

Claim 19 recites:

"*19. A method performed in response to execution of a first instruction, comprising:*

storing only a plurality of non-contiguous groups of source bits into a plurality of non-contiguous groups of destination storage locations in response to the execution of the first instruction, ***in which the first instruction implicitly indicates that the plurality of non-contiguous groups of source bits are to be stored into the plurality of non-contiguous groups of destination storage locations****; and*

duplicating bits from the plurality of non-contiguous groups of source bits into groups of destination storage locations adjacent to the non-contiguous groups of destination storage locations in response to the execution of the first instruction ***which implicitly indicates that the plurality of non-contiguous groups of source bits are to be duplicated***".

As understood by Applicants, Abdallah does not disclose these limitations or render them obvious. For example, as understood by Applicants, Abdallah does not disclose or render obvious "*storing only a plurality of non-contiguous groups of source bits into a plurality of non-contiguous groups of destination storage locations in response to the execution of the first instruction,* ***in which the first instruction implicitly indicates that the plurality of non-contiguous groups of source bits are to be stored into the plurality of non-contiguous groups of destination storage locations****; and duplicating bits from the plurality of non-contiguous groups of source bits into groups of destination storage locations adjacent to the non-contiguous groups of destination*

storage locations in response to the execution of the first instruction ***which implicitly indicates that the plurality of non-contiguous groups of source bits are to be duplicated.***"

Abdallah discloses in part a single-source shuffle packed single instruction. Column 6, lines 43-55 of Abdallah discloses, "*FIG. 3E illustrates the operation of a single-source shuffle packed single instruction (SHUFPS) according to one embodiment of the invention. The shuffle operation 352 essentially performs a permutation on the data elements in the packed data item. The data elements of an operand 350 are shuffled to occupy any location of a result data item 354. In one embodiment, the operand 350 and the result data item 354 correspond to the same register or memory location. In the illustrative example of FIG. 3E, any of the four data elements A, B, C, and D of the operand 350 can be stored in any of the locations of the result 354. Some examples of the organization of the result data item 354 after this shuffle single operation are A A A A, A B D C, D C B A, A D A B*"

However, as understood by Applicants, Abdallah does not disclose or render obvious that "***the first instruction implicitly indicates that the plurality of non-contiguous groups of source bits are to be stored into the plurality of non-contiguous groups of destination storage locations***" and that the first instruction "***implicitly indicates that the plurality of non-contiguous groups of source bits are to be duplicated,***" in combination with the other claim limitations.

As understood by Applicants, the data elements from the source operand 350 to be shuffled to the result data item 354 would need to be **explicitly specified**. For example, the SHUFPS instruction may have an operand or an immediate to **explicitly specify** the data elements from the source operand 350 to be shuffled to the result data item 354, or the SHUFPS instruction may indicate a register that explicitly specifies the data elements from the source operand 350 to be shuffled to the result data item 354. In any event, Abdallah does not teach or suggest that the SHUFPS instruction "***implicitly indicates that the plurality of non-contiguous groups of source bits are to be stored into the plurality of non-contiguous groups of destination storage locations***"

and that the SHUFPS instruction "***implicitly indicates* that the plurality of non-contiguous groups of source bits are to be duplicated***,*" in combination with the other claim limitations.

Anticipation under 35 U.S.C. Section 102 requires every element of the claimed invention be identically shown in a single prior art reference.

For at least one or more of these reasons, claim 19, and its dependent claims, are believed to be allowable.

Claim 93 recites:

"*93. An apparatus comprising:*

a first storage area to store a plurality of non-contiguous groups of source bits; and

a core coupled with the first storage area, the core in response to execution of a first instruction to store only the plurality of non-contiguous groups of source bits which are implicitly indicated by the instruction into a plurality of non-contiguous groups of destination storage locations and to store duplicates of the plurality of non-contiguous groups of source bits into groups of destination storage locations adjacent to the non-contiguous groups of destination storage locations."

As understood by Applicants, Abdallah does not disclose these limitations or render them obvious. For example, as understood by Applicants, Abdallah does not disclose or render obvious "*the core in response to execution of a first instruction to store only the plurality of non-contiguous groups of source bits* ***which are implicitly indicated by the instruction*** *into a plurality of non-contiguous groups of destination storage locations and to store duplicates of the plurality of non-contiguous groups of source bits into groups of destination storage locations adjacent to the non-contiguous groups of destination storage locations.*" The discussion of claim 19 above is pertinent to this point. For at least one or more of these reasons, claim 93, and its dependent claims, are believed to be allowable.

Claim 110 recites:

"*A medium that is readable by an apparatus having a processor and having stored thereon a processor-executable instruction, which if executed by the processor, causes the processor to perform a method comprising:*

storing bits [31-0] of a source value into bit storage locations [63-32] and [31-0] of a destination register;

storing bits [95-64] of the source value into bit storage locations [127-96] and [95-64] of the destination register, ***wherein the instruction implicitly indicates the bits of the source value which are to be stored in the destination register.***"

As understood by Applicants, Abdallah does not disclose these limitations or render them obvious. For example, as understood by Applicants, Abdallah does not disclose or render obvious that "***the instruction implicitly indicates the bits of the source value which are to be stored in the destination register,***" in combination with the other claim limitations. The discussion of claim 19 above is pertinent to this point. For at least one or more of these reasons, claim 110, and its dependent claims, are believed to be allowable.

Claim 113 recites:

"*113. A medium that is readable by an apparatus having a processor and having stored thereon a processor-executable instruction, which if executed by the processor causes the processor to perform a method comprising:*

storing bits [63-32] of a source value into bit storage locations [31-0] and [63-32] of a destination register;

storing bits [127-96] of the source value into bit storage locations [127-96] and [95-64] of the destination register, ***wherein the instruction implicitly indicates the bits of the source value which are to be stored in the destination register.***"

As understood by Applicants, Abdallah does not disclose these limitations or render them obvious. For example, as understood by Applicants, Abdallah does not disclose or render obvious that "***the instruction implicitly indicates the bits of the source value which are to be stored in the destination register,***" in combination with the other claim limitations. The discussion of claim 19 above is pertinent to this point. For at least one or more of these reasons, claim 113, and its dependent claims, are believed to be allowable.

Claim 116 recites:

"*116. A medium that is readable by an apparatus having a processor and having stored thereon a processor-executable instruction, which if executed by the processor causes the processor to perform a method comprising:*

storing only bits [63-32] of a source value into bit storage locations [127-96] and [63-32] of a destination register;

storing only bits [31-0] of the source value into bit storage locations [31-0] and [95-64] of the destination register, ***wherein the instruction implicitly indicates the bits of the source value which are to be stored in the destination register.***"

As understood by Applicants, Abdallah does not disclose these limitations or render them obvious. For example, as understood by Applicants, Abdallah does not disclose or render obvious that "***the instruction implicitly indicates the bits of the source value which are to be stored in the destination register,***" in combination with the other claim limitations. The discussion of claim 19 above is pertinent to this point. For at least one or more of these reasons, claim 116, and its dependent claims, are believed to be allowable.

Claim 119 recites:

"*119. A medium that is readable by an apparatus having a processor and having stored thereon a processor-executable instruction, which if executed by the processor, causes the processor to perform a method comprising:*

storing bits [31-0] of a source value into bit storage locations [31-0] of a destination register;

duplicating bits from the bit storage locations [31-0] to bit storage locations [63-32] of the destination register;

storing bits [95-64] of the source value into bit storage locations [95-64] of the destination register; and

duplicating bits from the bit storage locations [95-64] to bit storage locations [127-96] of the destination register, ***wherein the instruction implicitly indicates the bits of the source value which are to be stored in the destination register.***"

As understood by Applicants, Abdallah does not disclose these limitations or render them obvious. For example, as understood by Applicants, Abdallah does not disclose or render obvious that "***the instruction implicitly indicates the bits of the source value which are to be stored in the destination register,***" in combination with the other claim limitations. The discussion of claim 19

above is pertinent to this point. For at least one or more of these reasons, claim 119, and its dependent claims, are believed to be allowable.

Claim 120 recites:

"*120. A medium that is readable by an apparatus having a processor and having stored thereon a processor-executable instruction, which if executed by the processor causes the processor to perform a method comprising:*

storing bits [63-32] of a source value into bit storage locations [63-32] of a destination register;

duplicating bits from the bit storage locations [63-32] to bit storage locations [31-0] of the destination register;

storing bits [127-96] of the source value into bit storage locations [127-96] of the destination register; and

duplicating bits from the bit storage locations [127-96] to bit storage locations [95-64] of the destination register, ***wherein the instruction implicitly indicates the bits of the source value which are to be stored in the destination register.***"

As understood by Applicants, Abdallah does not disclose these limitations or render them obvious. For example, as understood by Applicants, Abdallah does not disclose or render obvious that "***the instruction implicitly indicates the bits of the source value which are to be stored in the destination register***," in combination with the other claim limitations. The discussion of claim 19 above is pertinent to this point. For at least one or more of these reasons, claim 120, and its dependent claims, are believed to be allowable.

Claim 101 recites:

"*101. A system comprising:*

a memory to store a plurality of instructions;

a processor to fetch a first instruction from the memory, wherein the first instruction, if executed by the processor, is to cause the processor to store only a plurality of non-contiguous groups of source bits ***which are not explicitly specified through the first instruction*** *into a plurality of non-contiguous groups of destination storage locations and to store duplicates of the plurality of non-contiguous groups of source bits into groups of destination storage locations adjacent to the non-contiguous groups of destination storage locations.*"

As understood by Applicants, Abdallah does not disclose these limitations or render them obvious. For example, as understood by Applicants, Abdallah does not disclose or render obvious that "*a processor to fetch a first instruction from the memory, wherein the first instruction, if executed by the processor, is to cause the processor to store only a plurality of non-contiguous groups of source bits* ***which are not explicitly specified through the first instruction*** *into a plurality of non-contiguous groups of destination storage locations and to store duplicates of the plurality of non-contiguous groups of source bits into groups of destination storage locations adjacent to the non-contiguous groups of destination storage locations.*" The discussion of claim 19 above is pertinent to this point. For at least one or more of these reasons, claim 101, and its dependent claims, are believed to be allowable.

35 U.S.C. §103(a) Rejection - Abdallah

Claims 107, 108, 121, and 123 have been rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Abdallah. Without admitting that these references could or should be combined, the Applicants respectfully submit that the present claims are allowable over Abdallah.

Claims 107 and 108 depend from independent claim 101. Claims 121 and 123 depend from independent claim 19. As discussed above, Abdallah does not disclose or render obvious the limitations of claim 19 or 101. Accordingly, Applicants respectfully submit that claims 19 and 101 are allowable over Abdallah. Dependent claims 107, 108, 121, and 123 are believed to be allowable for at least this reason, as well as for the recitations set forth in each of these dependent claims.

New Independent Claims Also Believed to be Allowable

Claim 135 recites:

"*135. An apparatus comprising:*
a register to store source bits;

a core coupled with the register, the core in response to execution of a first instruction to store a plurality of non-contiguous groups of the source bits, ***which are not explicitly specified through the first instruction****, into a plurality of non-contiguous groups of destination storage locations of a second register and to store duplicates of the plurality of non-contiguous groups of the source bits into groups of destination storage locations of the second register adjacent to the non-contiguous groups of destination storage locations.*"

As understood by Applicants, Abdallah does not disclose these limitations or render them obvious. For example, as understood by Applicants, Abdallah does not disclose or render obvious that "*a core coupled with the register, the core in response to execution of a first instruction to store a plurality of non-contiguous groups of the source bits,* ***which are not explicitly specified through the first instruction****, into a plurality of non-contiguous groups of destination storage locations of a second register and to store duplicates of the plurality of non-contiguous groups of the source bits into groups of destination storage locations of the second register adjacent to the non-contiguous groups of destination storage locations.*" For at least one or more of these reasons, claim 135 is believed to be allowable.

Claim 136 recites:

"*136. An apparatus comprising:*

a plurality of registers;

a core coupled with the registers, the core in response to a first instruction, ***which indicates operands consisting of a single source operand and a single destination operand****, to store a plurality of non-contiguous groups of source bits of the source operand into a plurality of non-contiguous groups of destination storage locations of the destination operand and to store duplicates of the plurality of non-contiguous groups of the source bits into groups of destination storage locations of the destination operand adjacent to the non-contiguous groups of destination storage locations.*"

As understood by Applicants, Abdallah does not disclose these limitations or render them obvious. For example, as understood by Applicants, Abdallah does not disclose or render obvious that "*a core coupled with the registers, the core in response to a first instruction,* ***which indicates operands consisting of a single source operand and a single destination operand****, to store a plurality of non-contiguous groups of source bits of the source operand into a plurality of non-*

contiguous groups of destination storage locations of the destination operand and to store duplicates of the plurality of non-contiguous groups of the source bits into groups of destination storage locations of the destination operand adjacent to the non-contiguous groups of destination storage locations." For at least one or more of these reasons, claim 136 is believed to be allowable.

Claim 137 recites:

"*137. An apparatus comprising:*

a plurality of registers; and

a core coupled with the registers, the core in response to a first instruction to:

store bits [31-0] of a source, ***which are not explicitly specified through the first instruction,*** *into bit storage locations [63-32] and [31-0] of a destination register; and*

storing bits [95-64] of the source, ***which are not explicitly specified through the first instruction,*** *into bit storage locations [127-96] and [95-64] of the destination register.*"

As understood by Applicants, Abdallah does not disclose these limitations or render them obvious. For example, as understood by Applicants, Abdallah does not disclose or render obvious that "*a core coupled with the registers, the core in response to a first instruction to: store bits [31-0] of a source,* ***which are not explicitly specified through the first instruction,*** *into bit storage locations [63-32] and [31-0] of a destination register; and storing bits [95-64] of the source,* ***which are not explicitly specified through the first instruction,*** *into bit storage locations [127-96] and [95-64] of the destination register.*" For at least one or more of these reasons, claim 137 is believed to be allowable.

Claim 138 recites:

"*138. An apparatus comprising:*

a plurality of registers; and

a core coupled with the registers, the core in response to a first instruction to:

store bits [63-32] of a source, ***which are not explicitly specified through the first instruction,*** *into bit storage locations [31-0] and [63-32] of a destination register; and*

store bits [127-96] of the source, ***which are not explicitly specified through the first instruction,*** *into bit storage locations [127-96] and [95-64] of the destination register.*"

As understood by Applicants, Abdallah does not disclose these limitations or render them obvious. For example, as understood by Applicants, Abdallah does not disclose or render obvious that "*a core coupled with the registers, the core in response to a first instruction to: store bits [63-32] of a source,* ***which are not explicitly specified through the first instruction,*** *into bit storage locations [31-0] and [63-32] of a destination register; and store bits [127-96] of the source,* ***which are not explicitly specified through the first instruction,*** *into bit storage locations [127-96] and [95-64] of the destination register.*" For at least one or more of these reasons, claim 138 is believed to be allowable.

Claim 139 recites:

"*A processor comprising:*

a front end to fetch instructions including a first instruction, a second instruction, and a third instruction, wherein each of the first, second, and third instructions is a different type of instruction; and

a core coupled with the front end to execute the instructions including the first instruction, the second instruction, and the third instruction, wherein

the core is responsive to the first instruction, instruction, which indicates a first source and a first destination register, to store bits [31-0] of the first source into bit storage locations [63-32] and [31-0] of the first destination register and to store bits [95-64] of the first source into bit storage locations [127-96] and [95-64] of the first destination register,

the core is responsive to the second instruction, which indicates a second source and a second destination register, to store bits [63-32] of the second source into bit storage locations [31-0] and [63-32] of the second destination register and to store bits [127-96] of the second source into bit storage locations [127-96] and [95-64] of the second destination register, and

the core is responsive to the third instruction, which indicates a third source and a third destination register, to store bits [63-32] of the third source into bit storage locations [127-96] and [63-32] of the third destination register and to store bits [31-0] of the third source into bit storage locations [31-0] and [95-64] of the third destination register."

As understood by Applicants, Abdallah does not disclose these limitations or render them obvious. Accordingly, claim 139, and its dependent claims, are believed to be allowable.

Conclusion

In view of the foregoing, it is believed that all claims now pending patentably define the subject invention over the cited art of record and are in condition for allowance. Applicants respectfully request that the rejections be withdrawn and the claims be allowed at the earliest possible date.

Request For Telephone Interview

The Examiner is invited to call Brent E. Vecchia at (303) 740-1980 if there remains any issue with allowance of the case.

Request For An Extension Of Time

The Applicants respectfully petition for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17 for such an extension.

Charge Our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

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Dated: May 5, 2010

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